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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,772	08/01/2005	Christopher Rodd Speirs	CH02 0021 US	4888

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EXAMINER	
ABDIN, SHAHEDA A	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,772	SPEIRS ET AL.	
	Examiner	Art Unit	
	SHAHEDA A. ABDIN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7 and 9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7 and 9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment field on 06/23/2009 has been entered and considered by Examiner.

Claim Objections

2. Claims 13-14 are objected to because of the following informalities: Claims 13 and 14 depends on canceled claim 4 which is improper. The dependency of the claims 13 and 14 should be changed to claim 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-7, 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta (US. Patent No: 20010033278 A1) in view of (Morita (US Patent No: 7079122 B1, see the IDS).

Regarding claim 9:

Ohta teaches the row drive circuit (3) for controlling n rows of a display device (1) that is operable in a partial mode ([0026-0027]), the row drive circuit (3) comprising :

a shift register (32) having n stages (e.g. 32g, 32d) and n outputs (output from 32g and 32d) and

a logic function (i.e. Flip-flop 37c) connected in front of each of the n outputs of the shift register (see the illustration in Fig. 3, the row driver circuit (3) is including a shift register 32 and logic function e.g. Flip-flop 37 is connected in front of each of the row output e.g. OG1, OG2....), the logic function deactivate n outputs (i.e. respective row output for non-display portion and display portion) of the shift register in dependence on the partial mode responsive to and during one or more pulses of a first control signal (e.g. GSP, GCNT1/2, control signal from a logic section, see Fig. 2) (also see [0028, 0032-0035]) by preventing (stop the voltage signal for **unscanned area, [0058] and [0060]]**) the n outputs of the shift register from driving the n rows (i.e. rows corresponding to the non display portion) of the display device (1) (note the signals are outputted from the shift register (i.e. 32) in accordance with the logic function (i.e. 37) to respective scanning lines and has a partial display function for a non-image area and an image display area that means the logic function (37) configured to prevent the shift register's output not to be displayed in respective scanning lines in the partial mode in the row drive circuit [0013] and Fig. 2) (see the illustration in Fig. 3, also see [0033-0035]).

Note that Ohta teaches output of the shift register are activated consecutively in dependence on pulses of a clock signal, but Ohta does not disclose frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal.

However, Morita in the same field of endeavor discloses frequency of the pulses of a clock signal (CLK) increases during the one or more pulses (i.e. one or more pulses in display are during time T1) of the first control signal (signal from logic section, see Fig. 11, column 14, lines 45-67, and column 15, lines 33-67).

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of increasing the frequency of a clock signal during one or more pulses of the first control signal (signal from logic section) as taught by Morita in to the scan driver of Ohta so that frequency of the pulses of the clock signal could be increased during the one or more pulses of the first control signal. In this configuration the system would provide a high efficient display device with improved image quality (Morita, abstract).

Regarding claim 12:

Ohta teaches a method (in Fig. 1-6) of realizing a partial mode (display divided in to non-display portion and display portion) of a display device, the display device controlled by a circuit arrangement that includes a row drive circuit (i.e. 3)

for driving n rows (i.e. OG1-OGl) and a column drive circuit (2) for supplying column voltages to m columns []0026-0028], the method comprising:

sequentially (line by line) providing an enable signal (GSP) to each row from 1 to n (OG1-OGl) in response to pulses of a clock signal (see Fig. 2) ([0032-0033]);

supplying (supplying through the column driver 2) the column voltages to the m columns for displaying corresponding picture data ([0031]). ,

deactivating all row outputs (deactivating all row outputs in non display portion) of a first row (row for the non display portion) of the row drive circuit (3) in response to a pulse of a first control signal (GCNT1/2) indicating that a first plurality of rows are not to be displayed in the partial mode of the display device (see Fig. 2, [0017], [0051]), and by preventing the row outputs of the first plurality of rows from driving the display device, (stop the voltage signal for unscanned area, [0058] and [0060]]) during the pulse of the first control signaland

activating all row outputs (activating all row outputs in display portion) of one or more rows subsequent to the first plurality of rows, in response to the enable signal (GSP) and the end of the first control signal pulse (GCNT1/2), indicating that the one or more rows are to be displayed in the partial mode ([0060], see Fig. 2).

Note that Ohta does not disclose frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal.

However, Morita in the same field of endeavor discloses frequency of the pulses of a clock signal (CLK) increases during the one or more pulses (i.e. one or more pulses in display are during time T1) of the first control signal (signal from logic section, see Fig. 11, column 14, lines 45-67, and column 15, lines 33-67).

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of increasing the frequency of a clock signal during one or more pulses of the first control signal (signal from logic section) as taught by Morita in to the scan driver of Ohta so that frequency of the pulses of the clock signal could be increased during the one or more pulses of the first control signal. In this configuration the system would provide a high efficient display device with improved image quality (Morita, abstract).

Regarding claim1:

Ohata in Fig. 2 teaches a circuit arrangement for controlling a display device (1) which can be operated in a partial mode (display divided in to non-display portion and display portion) [0026], the circuit arrangement comprising:

a row drive circuit (3) for driving n rows (OG1-OGl) of the display device (1) sequentially (line by line) from 1 to n, the row drive circuit responsive to a row enable signal (i.e. GSP) that is provided to each row from 1 to n ([0028]); and

a column drive circuit (i.e. 2) for driving m columns (data signal lines) of the display device (i.e. 1), by supplying column voltages to the m columns [003], the column voltages corresponding to picture data (image data) to be displayed as pixels of the controlled row [0027-0028], characterized in that a logic function (logic function from

control IC 4, note that controller 4 is interpreted as a control logic which function is interpreting as a logic function; the display portion and non display portions are set in advanced by the control IC 4, [0047]) is included in the row drive circuit (3) in front of row outputs (note that the gate driver 3 including a control logic section 31 which is corresponding to controller IC4 is placed in front of row output) ([0033-0034]), the logic function configured and arranged to respond to a first control signal, (i.e. GCNT1/2 corresponding to display scanning signal or display 'ON' signal), having one or more pulses indicative of whether or not the partial mode is to be implemented (apply) [0036], is supplied.

Note that Ohta teaches all of the limitation as recited in claim, but Ohta does not explicitly discloses the limitations "first control signal achieving a deactivation/activation of **by preventing one or more of the row outputs from driving one or more of the rows** in response to the row enable signal (GSP) in dependence on the partial mode", such limitation are merely would have been obvious in the system of **"Ohta"**. The limitations do not define a patentably distinct invention over that in **"Ohta"** since the invention as a whole and **"Ohta"** are directed to first control signal (GCNT1/2) achieving a deactivation/activation (i.e. deactivate row outputs to the Non-display area while activating the row outputs to the display area) of by preventing the at least one row output from driving the row in response to the row enable signal (GSP) in dependence on the partial mode ([0038-0039]). Therefore, **"Ohta"** would have been a matter of obvious choice to one of ordinary skill in the art to acquire the limitations "first control

signal achieving a deactivation/activation of **by preventing one or more of the row outputs from driving the row** in response to the row enable signal (GSP) in dependence on the partial mode". In this configuration the system would provide an optimum output to the display device, thereby reducing power consumption in the scanning signal line driving section (Ohta, [0017]).

the row drive circuit (3) comprises a shift register (3) which has n stages (e.g. 32g, 32d) and n outputs (output from 32g and 32d), and in that a second control signal (i.e. control signal from GCK) can be supplied to the shift register (32) at an input thereof for controlling the consecutive rows 1 to n (i.e. gate lines OG1-OGl), which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal and wherein the logic function (37) is connected between the n outputs of the shift register (i.e. output from the shift register 32) and the n rows (e.g. OG1, OG2) of the display, the logic function configured to prevent ((stop the voltage signal for **unscanned area, [0058] and [0060]]**)) the n outputs of the shift register from driving any of the n rows of the display responsive to the first control signal (note the signals are outputted from the shift register (i.e. 32) in accordance with the logic function (i.e. 37) to respective scanning lines and has a partial display function for a non-image area and an image display area that means
the logic function (37) configured to prevent the shift register's output not to be displayed in respective scanning lines in the partial mode in the row drive circuit [0013] and Fig. 2) (see the illustration in Fig. 3, also see [0033-0035]).

Note that Ohta does not disclose frequency of the pulses of the clock signal increases during the one or more pulses of the first control signal.

However, Morita in the same field of endeavor discloses frequency of the pulses of a clock signal (CLK) increases during the one or more pulses (i.e. one or more pulses in display are during time T1) of the first control signal (signal from logic section, see Fig. 11, column 14, lines 45-67, and column 15, lines 33-67).

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of increasing the frequency of a clock signal during one or more pulses of the first control signal (signal from logic section) as taught by Morita in to the scan driver of Ohta so that frequency of the pulses of the clock signal could be increased during the one or more pulses of the first control signal. In this configuration the system would provide a high efficient display device with improved image quality (Morita, abstract).

Regarding claim 2:

Ohta teaches the logic function (e.g. 37b, 37d) is connected in front of each row output (i.e. in front of row lines e.g. OG1-OGl) (see Fig. 3).

Regarding claim 3:

Ohta teaches the logic function is realized as an AND gate (AND circuit 37a) [0044].

Regarding claim 5:

Ohta teaches the first control signal (GCNT1/2 corresponding to display scanning signal) is capable of switching off (that is changing "ON' to 'OFF') all n row outputs by means of the logic function during control of a line that is not to be displayed in the partial mode (i.e. non display portion e.g. 1b, 1c) ([0030-0034], and [0051]).

Regarding claim 6:

Ohta teaches that control logic (IC4) in the column drive circuit generates the first control signal (signal from GCNT1/2 corresponding to scan "ON" signal) in dependence on the partial mode and supplies the first control signal to the row drive circuit ([([0030-0034], and [0051])]).

Regarding claim 7:

Ohta teaches the column drive circuit (2) supplies no column voltages to the m columns (i.e. deactivate the operation of the source driver) in a case of a line that is not to be displayed ([0049]).

Regarding claim 10:

Ohta teaches that a display device (1) comprising a circuit arrangement (see the illustration in Fig. 1-4).

Regarding claim 11:

An electronic appliance (I.e. LCD in Fig. 2) comprising a display device (1) ([0027]).

Regarding claim 13:

Ohta teaches wherein each of the stages includes a flip-flop (e.g. 32) (see the illustration in Fig. 3).

Regarding claim 14:

Ohta discloses the first control signal (signal from GCNT1/2 corresponding to "ON" signal) overrides (make ineffective) the second control signal (i.e. signal from GCK) ([0036]) (note that the second control signal i.e. GCK is applied to the output lines (i.e. gate lines); the shift register control block 32 signaled by the gate start pulse from the control logic section 31, and output the scanning signal for outputting for outputting the ON signal. Thus, the first control signal override the second control signal from GCK).

Response to Arguments

5. Applicant's arguments, with respect to claims1-3, 5-7, and 9-14 have been considered but are moot in view of new ground of rejection.

In view of amendment the reference of Morita (US Patent No: 7079122, see the IDS) has been added.

Inquiry

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Shaheda Abdin** whose telephone number is (571) 270-1673.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard HJerpe** could be reached at (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pari-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shaheda Abdin

05/07/2010

/Richard Hjerpe/

Supervisory Patent Examiner, Art Unit 2629